Fully Digital-controlled Power Supply Control IC with Interleaved Totem-pole Bridgeless PFC Circuit

MD6753

Data Sheet

Description

The MD6753 is a fully digital-controlled power supply IC that controls interleaved totem-pole bridgeless PFC. Interleaving control in the critical conduction mode reduces input/output ripple current and switching loss, and the IC can achieve high-efficient, yet low-noise power systems.

Features

- Fully Digital-controlled PFC Circuit
- Interleaved Totem-pole PFC Control
- Critical Conduction Mode (CRM) Control
- Bridgeless PFC Circuit
- High Efficiency in All Load Ranges Achieved by Synchronous Rectification and Intermittent Operation at Light Load
- Soft Start
- Protections Include:

- AC Power Supply Input Undervoltage Lockout
- AC Power Supply Input Off-state Detection
- PFC Output Undervoltage Protection (PFC_UVP)
- PFC Output Overvoltage Protection (PFC_OVP)
- PFC Overcurrent Protection (PFC_OCP)
- PFC Overload Protection (PFC_OLP)
- AC Regeneration Side High-side Driver Undervoltage Lockout
- VCC Pin Overvoltage Protection (VCC_OVP)
- Thermal Shutdown (TSD)

Package

SOP28

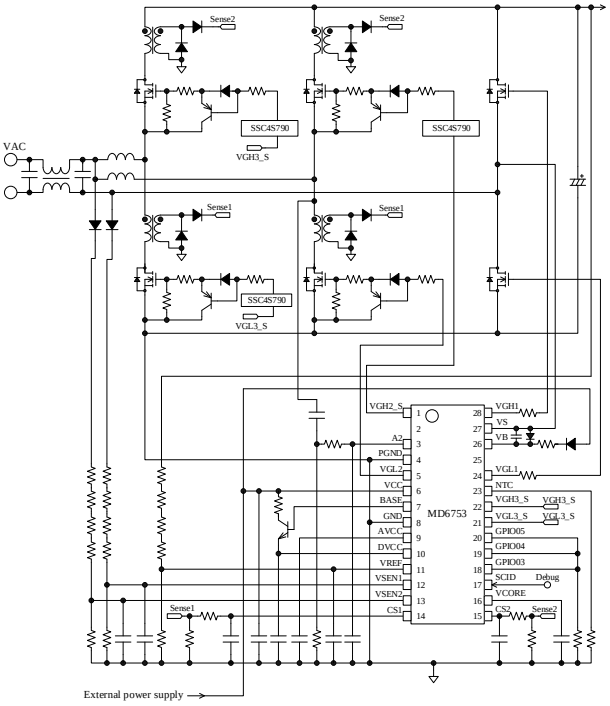
Not to scale

Applications

For devices requiring high power supplies (1 kW or more) such as:

- Audiovisual Equipment
- Office Automation Equipment (e.g., Server, Multifunction Printer)
- Industrial Equipment
- Communication Equipment

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C. Surge withstand capability (HBM) of the MD6753 is guaranteed up to 2000 V. Note that the following pins are guaranteed to withstand surges up to 1000 V: 26, 27, 28.

Parameter	Symbol	Pin	Rating	Unit
VGH2_S Pin Voltage[6]	V_{GH2_S}	1−8	−0.3 to 5.5	V
VGH2_S Pin Current[6]	I_{GH2_S}	1−8	−4.0 to 4.0	mA
A2 Pin Voltage	V_{A2}	3−8	−2.0 to 6.0	V
PGND Pin Voltage	V_{PGND}	4−8	−0.3 to 0.3	V
VGL2 Pin Voltage	V_{GL2}	5−8	−0.3 to V_{CC} + 0.3	V
VGL2 Pin Voltage ($t_W \leq 50$ ns)	$V_{GL2(PULSE)}$	5−8	−1.5	V
VCC Pin Voltage	V_{CC}	6–8	−0.3 to 20	V
BASE Pin Voltage	V_{BASE}	7–8	−0.3 to 6.0	V
AVCC Pin Voltage[1][2]	V_{AVCC}	9–8	−0.3 to 3.6	V
DVCC Pin Voltage[2]	V_{DVCC}	10–8	−0.3 to 3.6	V
VREF Pin Voltage[3]	V_{REF}	11–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VSEN1 Pin Voltage[3]	V_{SEN1}	12−8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VSEN2 Pin Voltage[3]	V_{SEN2}	13−8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
CS1 Pin Voltage[3]	V_{CS1}	14–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
CS2 Pin Voltage[3]	V_{CS2}	15–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VCORE Pin Voltage[4]	V_{CORE}	16–8	−0.3 to 2.0[5]	V
SCID Pin Voltage	V_{SCID}	17–8	−0.3 to 5.5	V
GPIO03 Pin Voltage[6]	V_{GPIO03}	18–8	−0.3 to 5.5	V
GPIO03 Pin Current[6]	I_{GPIO03}	18–8	−4.0 to4.0	mA
GPIO04 Pin Voltage[6]	V_{GPIO04}	19–8	−0.3 to 5.5	V
GPIO04 Pin Current[6]	I_{GPIO04}	19–8	−4.0 to 4.0	mA
GPIO05 Pin Voltage[6]	V_{GPIO05}	20–8	−0.3 to 5.5	V
GPIO05 Pin Current[6]	I_{GPIO05}	20–8	−4.0 to 4.0	mA
VGL3_S Pin Voltage[6]	V_{GL3_S}	21−8	−0.3 to 5.5	V
VGL3_S Pin Current[6]	I_{GL3_S}	21−8	−4.0 to 4.0	mA
VGH3_S Pin Voltage[6]	V_{GH3_S}	22−8	−0.3 to 5.5	V
VGH3_S Pin Current[6]	I_{GH3_S}	22−8	−4.0 to 4.0	mA
NTC Pin Voltage	V_{NTC}	23–8	−6.0 to 6.0	V
VGL1 Pin Voltage	V_{GL1}	24–8	−0.3 to V_{CC} + 0.3	V
VB–VS Pin Voltage	V_{BS}	26–27	−0.3 to 20.0	V
VS Pin Voltage	V_S	27–8	−1 to 600 − V_B	V
VGH Pin Voltage	V_{GH}	28–8	V_S − 0.3 to V_B + 0.3	V
Operating Ambient Temperature	T_{OP}	—	−40 to 85	°C
Storage Temperature	T_{STG}	—	−40 to 125	°C
Junction Temperature	T_J	—	125	°C

[1] The AVCC pin is the 3.3 V power supply output pin dedicated for the internal LSI chip. Do not apply external voltage to this pin.
[2] Electric potential difference between the AVCC and DVCC pins should be maintained within ±0.3 V （t > 1 ms).
[3] Refers to an analog input pin for 3.3 V systems.
[4] The VCORE pin is the 1.8 V power supply output pin dedicated for digital circuits of the internal LSI chip. Do not apply external voltage to this pin.
[5] Should be rated from −0.3 V to 2.4 V when t < 1 ms (e.g., at startup).
[6] Refers to a digital output pin for 3.3 V systems.

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 17 V.

The checkmark in the Chg. column indicates that the item is software-changeable. In addition, the characteristic value in this column is a reference value.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
Startup Circuit, Circuit Current								
Operation Start Voltage	$V_{CC(ON)}$		6–8	10.0	11.0	12.0	V	
Operation Stop Voltage	$V_{CC(OFF)}$		6–8	7.4	8.3	9.2	V	
Circuit Current in Operation	$I_{CC(ON)}$		6–8	—	1.8	4.0	mA	
Circuit Current in Non-operation	$I_{CC(OFF)}$	V_{CC} = 9 V	6–8	—	0.5	1.0	mA	
VCC Pin Protection Release Threshold Voltage	$V_{CC(P.OFF)}$		6–8	7.4	8.3	9.2	V	
Circuit Current in Protection Operation	$I_{CC(P)}$	V_{CC} = 10 V	6–8	—	0.5	1.0	mA	
VCORE Pin Supply Voltage	V_{CORE}		16–8	1.72	1.80	1.88	V	
SCID Pin High Level Detection Voltage[1]	V_{SCID_IH}		22–8	2.0	—	—	V	
SCID Pin Low Level Detection Voltage[1]	V_{SCID_IL}		22–8	—	—	0.8	V	
3.3 V Analog Internal Regulator	V_{AVCC}		9–8	3.233	3.300	3.366	V	
3.3 V Digital Internal Regulator	V_{DVCC}		10–8	3.135	3.300	3.465	V	
External Transistor Drive Voltage for DVCC Pin	V_{BASE}	I_{BASE} = −1 mA	7–8	3.6	—	4.4	V	
VSEN Pin Input UVP Threshold Voltage	$V_{SEN(OFF)}$		12–8 13–8	0.43	0.47	0.50	V	✓
VSEN Pin Input UVP Release Voltage	$V_{SEN(ON)}$		12–8 13–8	0.52	0.56	0.60	V	✓
VSEN Pin AC Input Voltage Off-state Detection Voltage	$V_{SEN(AC\_OFF)}$		12–8 13–8	0.16	0.19	0.22	V	✓
Delay Time of VSEN Pin Input UVP Detection	$t_{VSEN(OFF)}$		12–8 13–8	9.5	10.0	10.5	ms	✓
Delay Time of VSEN Pin AC Input Voltage Off-state Detection	$t_{VSEN(AC\_OFF)}$		12–8 13–8	21.9	23.0	24.2	ms	✓
PFC Stage								
VGL1 Drive Current (Source)	$I_{GL1(SRC)}$	V_{CC} = 17 V, V_{GL1} = 0 V	24–8	—	−0.3	—	A	
VGL1 Drive Current (Sink)	$I_{GL1(SNK)}$	V_{CC} = 17 V, V_{GL1} = 17 V	24–8	—	0.55	—	A	
VGH1 Drive Current (Source)	$I_{GH1(SRC)}$	V_{CC} = 17 V, V_{GH1} = 0 V	28–8	—	−0.3	—	A	
VGH1 Drive Current (Sink)	$I_{GH1(SNK)}$	V_{CC} = 17 V, V_{GH1} = 17 V	28–8	—	0.55	—	A	
VGL2 Drive Current (Source)	$I_{GL2(SRC)}$	V_{CC} = 17 V, V_{GL2} = 0 V	5–8	—	−0.5	—	A	
VGL2 Drive Current (Sink)	$I_{GL2(SNK)}$	V_{CC} = 17 V, V_{GL2} = 17 V	5–8	—	1	—	A	

[1] Guaranteed by design.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
AC Regeneration Side High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		26–27	5.8	6.8	7.8	V	
AC Regeneration Side High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		26–27	5.4	6.4	7.4	V	
CS1 / CS2 Pin OCP Threshold Voltage (Low)	$V_{CS(LO)}$		14–8 15–8	1.556	1.618	1.677	V	✓
CS1 / CS2 Pin OCP Threshold Voltage (High)	$V_{CS(HI)}$		14–8 15–8	0.373	0.388	0.402	V	✓
Number of OVP Operation Times	$N_{OPP(AC)}$		—	—	32	—	Times	✓
VREF Pin Threshold Voltage for PFC Output Control	V_{REF}		11–8	2.121	2.205	2.285	V	✓
Minimum PFC On-time	$t_{ON(MIN)\_PFC}$		5–8	0.29	0.30	0.32	µs	✓
Maximum PFC On-time	$t_{ON(MAX)\_PFC}$		5–8	16.2	17.0	17.9	µs	✓
VREF Pin PFC_UVP Start Voltage	$V_{REF(UVD)}$		11–8	2.008	2.088	2.164	V	✓
VERF Pin PFC_UVP Oscillation Stop Voltage	$V_{REF(UVP)}$		11–8	1.061	1.103	1.143	V	✓
VREF Pin PFC_UVP Release Voltage	$V_{REF(UVP\_R)}$		11–8	0.531	0.552	0.572	V	✓
PFC_UVP Recovery Delay Time	$t_{(UVP\_R)}$		—	780.2	819.2	862.3	ms	✓
VREF Pin PFC_OVP Start Voltage	$V_{REF(OVD)}$		11–8	2.233	2.322	2.406	V	✓
VREF Pin PFC_OVP Oscillation Stop Voltage	$V_{REF(OVP)}$		11–8	2.262	2.352	2.437	V	✓
VREF Pin PFC_OVP Oscillation Stop Release Voltage	$V_{REF(OVP\_R)}$		11–8	2.209	2.297	2.381	V	✓
Auto-restart Protection								
Protection Recovery Time	t_{AR}		—	2860	3000	3160	ms	✓
Overvoltage Protection (OVP)								
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		6–8	18.1	19.0	19.7	V	
NTC								
NTC Pin Protection Threshold Voltage	V_{NTC}		23–8	1.29	1.35	1.40	V	✓
NTC Pin Pull-up Resistor	R_{NTC}		23–8	36	108	180	kΩ	
NTC Pin Offset Voltage[2]	V_{ANEX0}	V_{NTC} = 0 V	23–8	—	1.65	—	V	
Digital General-purpose I/O								
A2 Pin A2 Threshold Voltage (POS)	$V_{A2(POS)}$		3–8	−0.125	−0.130	−0.135	V	✓
A2 Pin A2 Threshold Voltage (NEG)	$V_{A2(NEG)}$		3–8	0.442	0.460	0.477	V	✓
A2 Pin Pull-up Resistor	R_{A2}		3–8	20	60	100	kΩ	
A2 Pin Offset Voltage[3]	$V_{A2(OFS)}$	V_{A2} = 0 V	3–8	—	0.6	—	V	
GPIO Pin High Level Detection Voltage	V_{IH}		[4]	2.0	—	—	V	
GPIO Pin Low Level Detection Voltage	V_{IL}		[4]	—	—	0.8	V	

[2] See Figure 3-2.
[3] See Figure 3-1.
[4] Refers to voltage between the GND pin and all the following pins: GPIO03, GPIO04, GPIO05.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
Digital Pull-up Resistor	R_{PUP}		(4)	20	60	100	kΩ	
Analog Pull-up Resistor (CS1, CS2)	R_{PUP2}		14–8 15–8	7.9	10.0	12.4	kΩ	
Input Leakage Current	I_L	V_{REF} = 0 V V_{SEN} = 0 V	11–8 12–8 13–8	−2	±1	2	μA	
GPIO Pin High Level Output Voltage	V_{OH4}	I_{OH} = −4 mA	(4)	2.4	—	—	V	
GPIO Pin Low Level Output Voltage	V_{OL4}	I_{OH} = 4 mA	(4)	—	—	0.4	V	
Clock Operation								
Internal IRC Oscillation Frequency	f_{IRC}		—	11.64	12.00	12.18	MHz	
Thermal Shutdown (TSD)								
TSD Operating Temperature(5)	$T_{J(TSD)}$		—	125	—	—	°C	
Thermal Characteristic								
Junction-to-Air Thermal Resistor	θ_{J-A}		—	—	—	85	°C/W	

(5) Guaranteed by design.

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.675	—	g

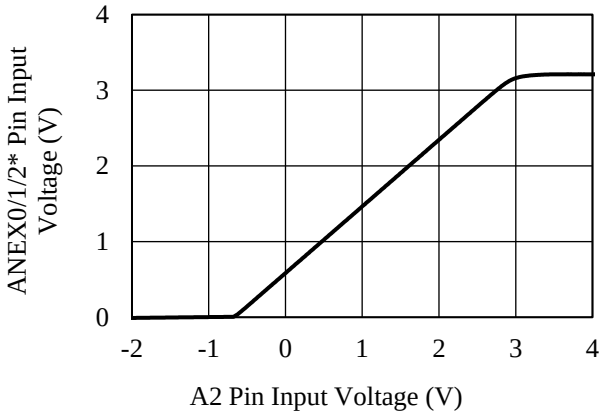


Figure 3-1. A2 Pin Offset

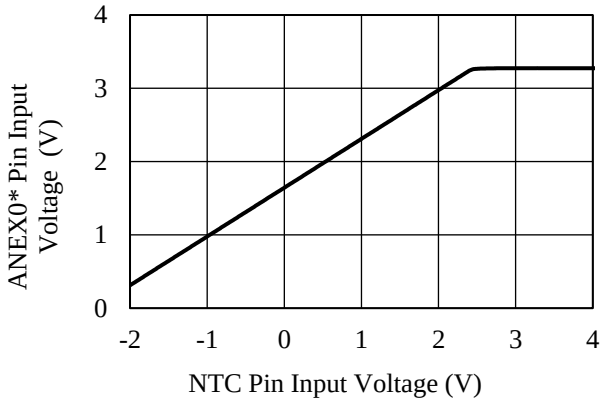
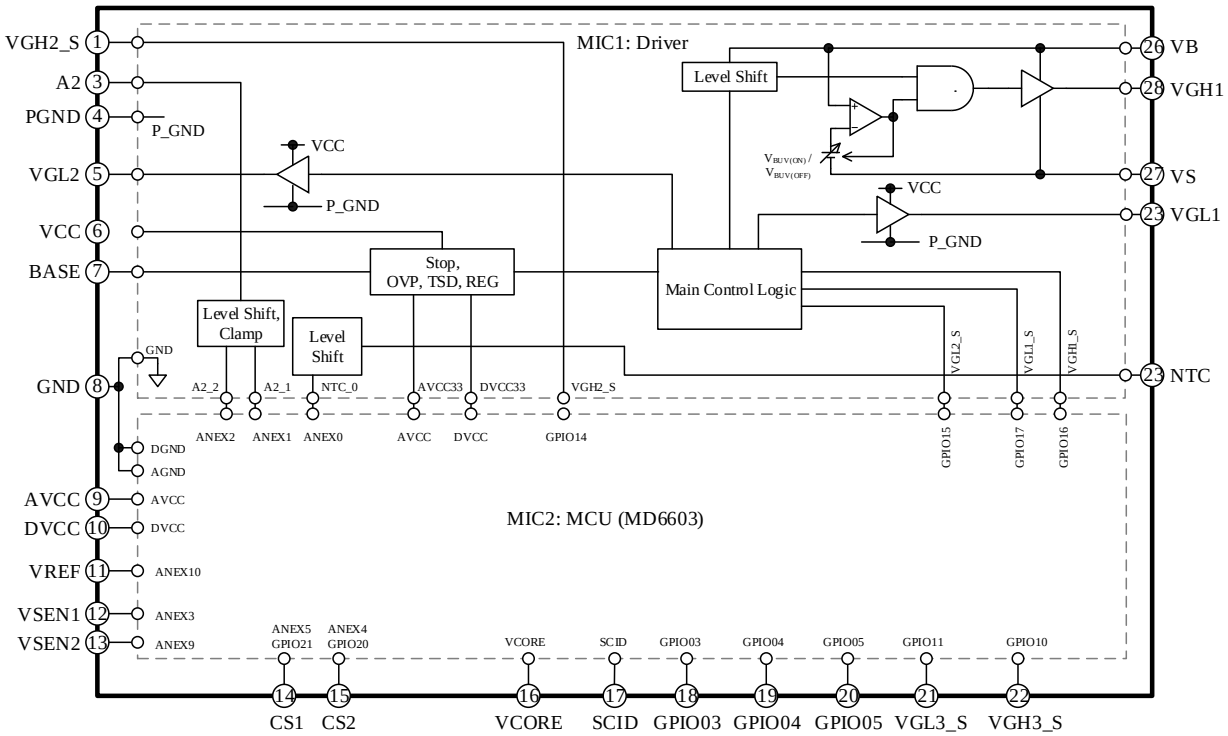


Figure 3-2. NTC Pin Offset

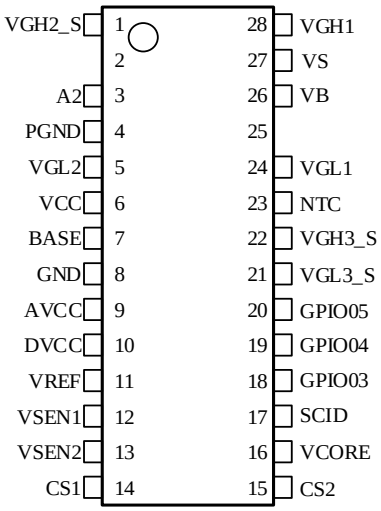
* Indicates voltages inside the IC; see the block diagram in Section 4.

4. Block Diagram



5. Pin Configuration Definitions

Top View



No.	Name	Description
1	VGH2_S	Master side high-side PWM signal output
2	—	Pin removed
3	A2	Analog input
4	PGND	Power ground
5	VGL2	Master side low-side gate drive output
6	VCC	Logic power supply input; VCC_OVP
7	BASE	External transistor base voltage output for the DVCC pin
8	GND	Ground
9	AVCC	3.3 V analog power supply
10	DVCC	3.3 V digital power supply
11	VREF	PFC constant voltage control signal input; PFC_UVP / PFC_OVP
12	VSEN1	Input voltage detection signal input 1
13	VSEN2	Input voltage detection signal input 2
14	CS1	PFC_OCP / PFC_OLP signal input 1 (Positive AC input)
15	CS2	PFC_OCP / PFC_OLP signal input 2 (Negative AC input)
16	VCORE	Capacitor connection for internal digital circuit supplies
17	SCID	Debugging pin (left open if not used)
18	GPIO03	General-purpose I/O pin
19	GPIO04	General-purpose I/O pin
20	GPIO05	General-purpose I/O pin
21	VGL3_S	Subordinate low-side PWM signal output
22	VGH3_S	Subordinate high-side PWM signal output
23	NTC	Analog input (External Shutdown Input)
24	VGL1	AC regeneration side low-side gate drive output
25	—	Pin removed
26	VB	Power supply input for AC regeneration side high-side gate drive with UVLO; VB_UVLO signal input
27	VS	Floating ground of AC regeneration side high-side driver
28	VGH1	AC regeneration side high-side gate drive output

Reference Internal Connection Symbols (MIC1–MIC2; see Section 4)

MIC1 (Driver)	MIC2 (MCU)	Transmission Signal
VGH2_S	GPIO14	Master side high-side PWM signal
VGL2_S	GPIO15	Master side low-side PWM signal
VGH1_S	GPIO16	AC regeneration side high-side PWM signal
VGL1_S	GPIO17	AC regeneration side low-side PWM signal
DVCC33	DVCC	3.3 V digital power supply pin
AVCC33	AVCC	3.3 V analog power supply pin
NTC_0	ANEX0	Level-shift signal 0 for the NTC pin
A2_1	ANEX1	Level-shift signal 1 for the A2 pin
A2_2	ANEX2	Level-shift signal 2 for the A2 pin

6. Typical Application

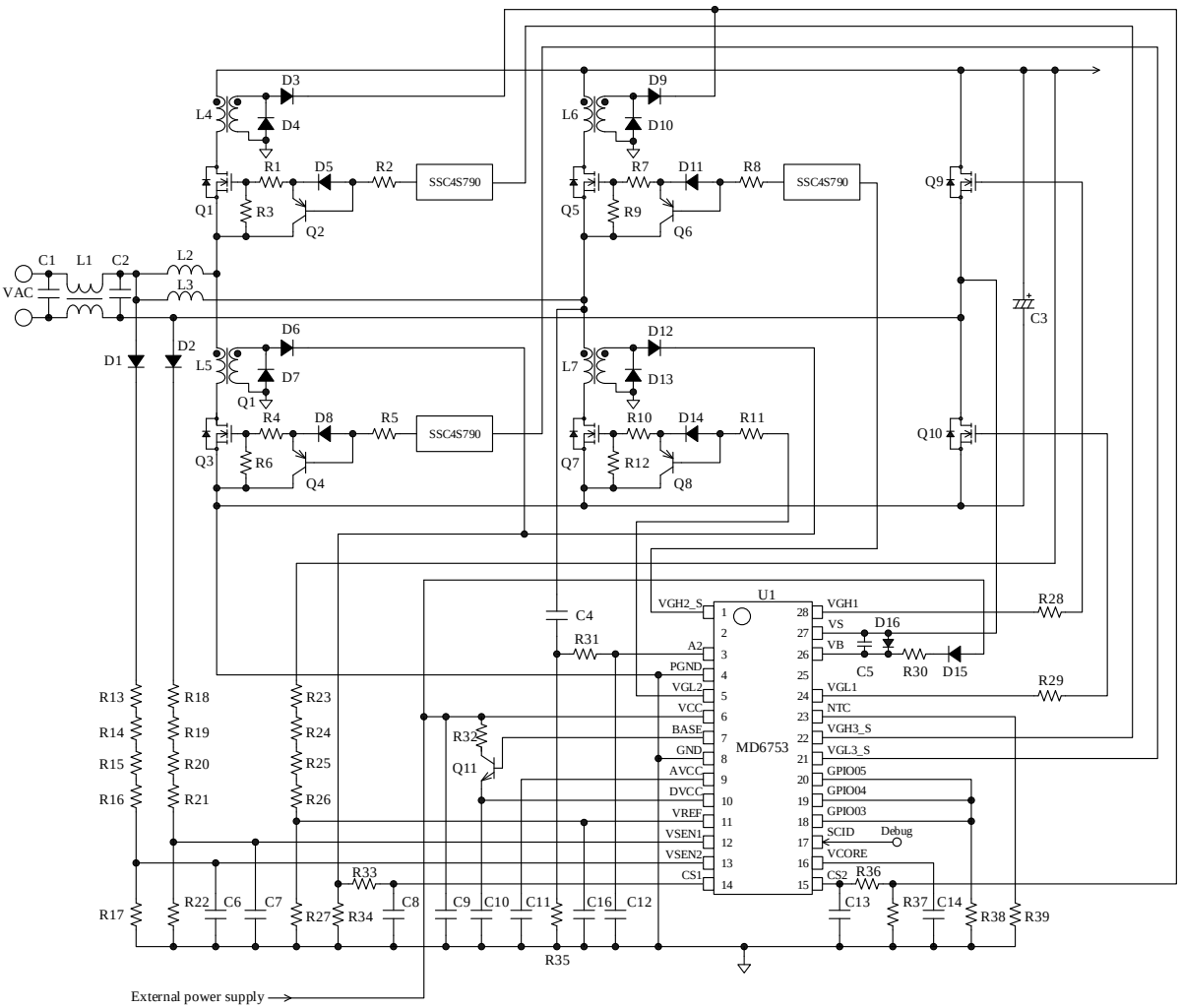
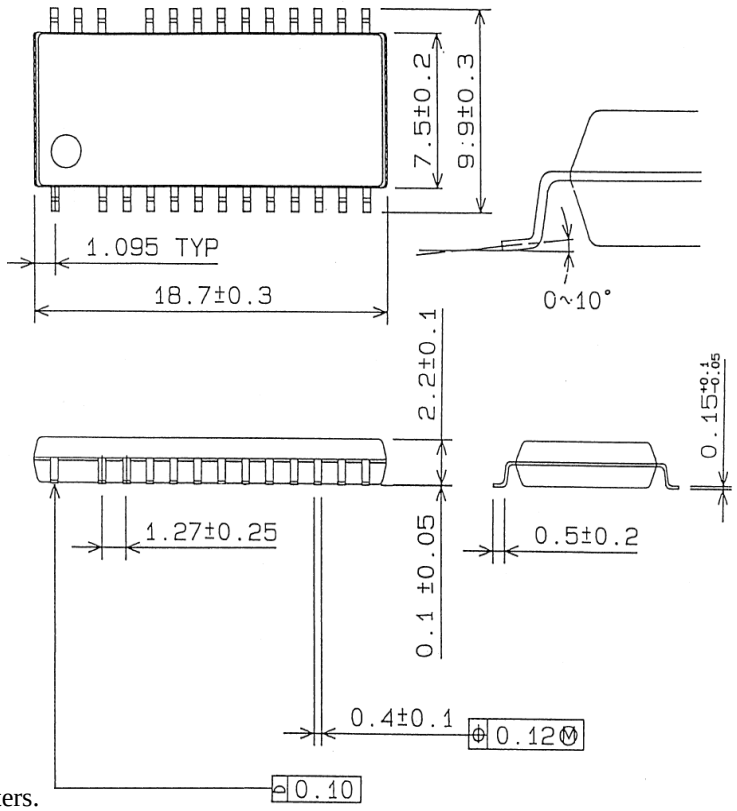


Figure 6-1. Typical Application

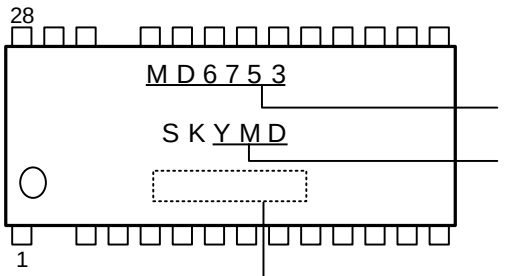
7. Physical Dimensions

● SOP28



NOTES:
● Dimension is in millimeters.
● Pb-free

8. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is the period of days represented by:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

9. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 2 and the electronic symbol names of the typical application in Section 6.

9.1. General Description

The MD6753 digitally controls a PFC circuit.

The PFC circuit embedded in the IC requires no input rectifier bridge for its own controlling. The PFC circuit, driven by critical conduction mode (CRM) in normal operation, is controlled with the frequencies suitable for applied input voltages and loads. By monitoring the output voltage of the PFC circuit with the VREF pin, the IC controls the VGL1, VGH1, VGL2, VGH2_S, VGL3_S, and VGH3_S pins on-time and provides regulated outputs.

Protections in the PFC stage include the overcurrent and overload protections, the overvoltage protection, and the undervoltage protection.

In addition to the protections above, the IC also has the following functions: the AC regeneration side high-side driver undervoltage lockout, the soft start function, the VCC pin overvoltage protection (to prevent secondary outputs from overvoltage), and the thermal shutdown.

9.2. Pin Descriptions

9.2.1. A2

This is the input pin for analog signals. The A2 pin is internally connected to the comparator and the AD converter. Leave this pin open if not used.

For more details, refer to the MD6603 data sheet.

9.2.2. GND and PGND

The GND pin is the logic ground pin of the IC; the PGND pin is the power ground pin where driving currents for an external power MOSFET flow through. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, extreme care should be taken in designing a PCB so that currents from the power ground do not affect these pins.

9.2.3. VGL1 and VGH1

These pins are the drive output pins for driving the AC regeneration side power MOSFETs. The VGL1 pin acts as a low-side driver, whereas the VGH1 pin acts as a high-side driver. Respective drive currents are defined as follows: the VGL1 Drive Current (Source), $I_{GL1(SRC)} = I_{GH1(SRC)} = -0.3$ A; the VGL1 Drive Current (Sink), $I_{GL1(SNK)} = I_{GH1(SNK)} = 0.55$ A.

9.2.4. VGL2, VGH2_S, VGL3_S, and VGH3_S

The VGL2 pin is the drive output pin for driving the master side low-side power MOSFET by interleaving control. Respective drive currents are defined as follows: the VGL2 Drive Current (Source), $I_{GL2(SRC)} = 0.5$ A; the VGL2 Drive Current (Sink), $I_{GL2(SNK)} = 1$ A.

The VGH2_S pin is the PWM signal output pin for driving the control IC for the master side high-side power MOSFET by interleaving control.

The VGL3_S pin is the PWM signal output pin for driving the control IC for the subordinate side low-side power MOSFET by interleaving control.

VGH3_S pin is the PWM signal output pin for driving the control IC for the subordinate side high-side power MOSFET by interleaving control.

The description hereafter holds up the peripheral circuit of Q1 as an example (but is also applicable to Q3, Q5, and Q7). To increase a rising speed of the gate at power MOSFET turn-off, connect the transistor Q2 as shown in Figure 9-1. Q2, D5, R1, and R2 should be adjusted based on the operation performance checked with an actual board, including a loss in the power MOSFET, gate waveform (e.g., ringing due to pattern layout), and EMI noise. To prevent malfunction caused by steep dv/dt at power MOSFET turn-off, connect R3, of about 10 kΩ to 100 kΩ, between the gate and source of the power MOSFET with a minimal length of traces.

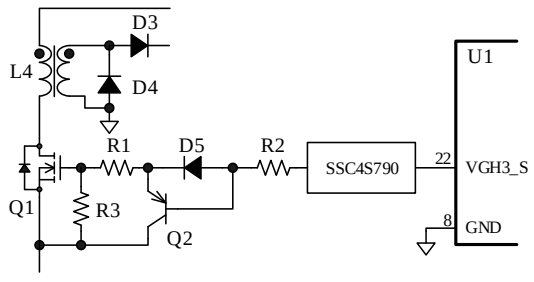


Figure 9-1. Q1 and Its Peripheral Circuit

9.2.5. VCC

This is the power supply pin for the built-in control MICs, and is connected to an external power supply. When the VCC pin voltage increases to $V_{CC(ON)}$ or more, the IC starts operating. When the VCC pin voltage decreases to $V_{CC(OFF)}$ or less, the IC stops operating. This sequence of operations is the VCC pin undervoltage lockout (VCC_UVLO). In addition to this function, the VCC pin also has the VCC pin overvoltage protection (VCC_OVP).

To prevent malfunction induced by supply ripples or other factors, connect the 0.01 µF to 0.1 µF ceramic capacitor, C9, between the VCC and GND pins, respectively, with a minimal length of traces.

9.2.6. DVCC and BASE

The DVCC pin is the internal 3.3 V digital power supply pin. As Figure 9-2 illustrates, the DVCC pin power is supplied from the external power supply through an external transistor. The BASE pin is connected to the base of this external transistor. To reduce noises on the DVCC pin, connect the capacitor C10 with a capacitance of about 0.1 µF to 1 µF.

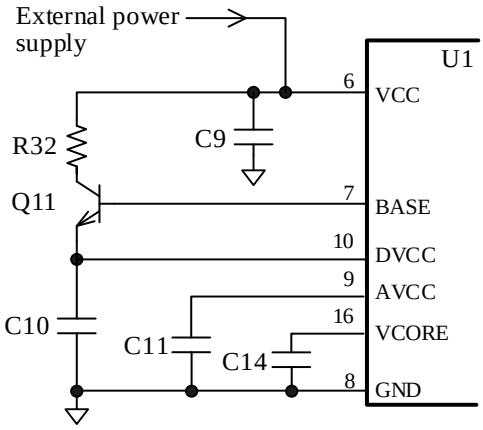


Figure 9-2. Power Stage and Its Peripheral Circuit

9.2.7. AVCC

The AVCC pin is the internal 3.3 V analog power supply pin. The capacitor C11 in Figure 9-2 should have a capacitance of about 0.1 µF to 1 µF. Do not connect anything but C11 to the AVCC pin.

9.2.8. VREF

As shown in Figure 9-3, the output voltage of the PFC stage, $V_{OUT(PFC)}$, divided by the detection resistors is applied to the VREF pin. Signals input to the VREF pin are used for the constant voltage control in the PFC stage, the overvoltage protection, and the undervoltage protection. $V_{OUT(PFC)}$ is determined by the detection resistors, R23 to R27, and can be calculated by the equation below:

$$V_{OUT(PFC)} = \left(\frac{R_{REF1}}{R_{REF2}} + 1\right) \times V_{REF} . \quad (1)$$

Where:

V_{REF} is the VREF pin threshold voltage (2.205),
R_{REF1} is the combined resistance of the resistors R23 to R26, and
R_{REF2} is the resistance of R27 (≈ 10 kΩ to 68 kΩ).

The resistors of R_{REF1} are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R_{REF1} with some serial resistors to reduce each applied voltage.

R27 should be adjusted based on the operation performance checked with an actual board, including a PFC output, overvoltage protection, and undervoltage protection.

To reduce switching noises, connect the capacitor C16 with a capacitance of about 1000 pF, as near as possible to the VREF pin.

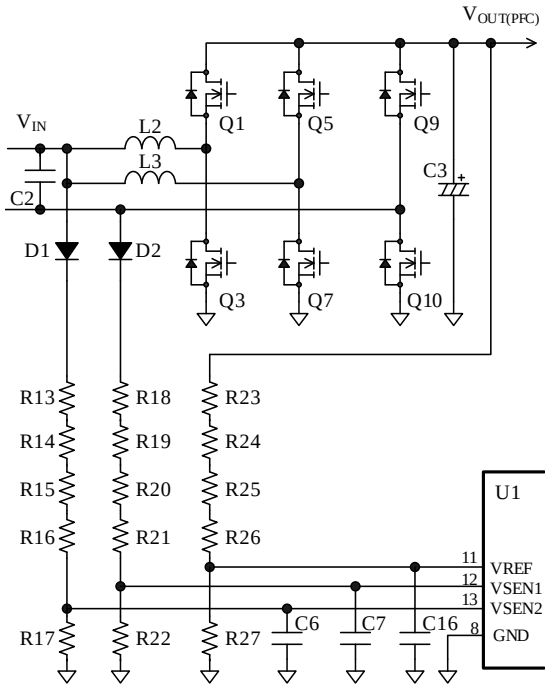


Figure 9-3. VREF and VSENx Pins and Their Peripheral Circuit

9.2.9. CS1 and CS2

These pins serve as a drain current detector of the power MOSFET in the PFC circuit. In the PFC circuit, which supports high-power applications, current through the power MOSFET is usually detected by the current transformers (L4 to L7) as in Figure 9-4. Then, a detection signal is input to the CSx pin. Current detection signals transmitted from the CSx pin are used for the protections against overcurrent and overload conditions. The CS1 and CS2 pins detect the turn-off timing of the power MOSFETs when the AC power input is positive and detect the turn-on timing when the AC power input is negative. As a result, the IC controls the PFC stage in the critical conduction mode.

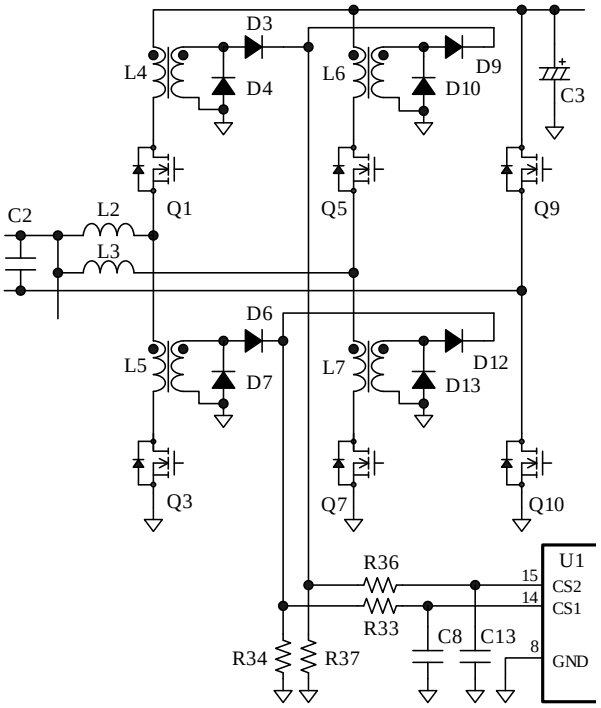


Figure 9-4. CSx Pins and Their Peripheral Circuit

9.2.10. VSEN1 and VSEN2

As shown in Figure 9-3, the input voltage, V_{IN}, divided by the detection resistors is applied to the VSENx pin. Signals input to the VSENx pin are used for the undervoltage lockout and the input voltage off-state detection.

9.2.11. VCORE

The VCORE pin is the internal 1.80 V power supply pin. The capacitor C14 should have a capacitance of 0.1 µF. Do not connect anything but C14 to the VCORE pin.

9.2.12. GPIO03 to GPIO05

These pins are the general-purpose I/O pins. For more details, refer to the MD6603 data sheet.

The GPIO04 pin has the AC power supply input off-state detection function, which outputs a signal at AC power supply cutoff. Connect the pull-down resistor, R38 (about 1 kΩ), to the logic ground, if not used.

9.2.13. SCID

This is the debugging pin. For detailed functional descriptions, such as software debugging, and software programming (erasing and writing) to the programs on the flash memory, refer to the MD6603 data sheet. Leave this pin open if not used.

9.2.14. NTC

This pin is used for analog input and external shutdown input. The NTC pin should be used within the range of absolute maximum ratings (see Section 1). When the NTC pin voltage increases to $V_{NTC(ON)}$ = 1.35 V or more, and remains in this condition for 1000 ms or longer, the oscillation operations of the VGH and VGL pins are stopped. After t_{AR} = 3000 ms or longer, the IC releases the protection operation and restarts to operate.

Connect the pull-down resistor, R39 (about 1 kΩ), to the logic ground, if not used.

9.2.15. VB and VS

The VB pin is the input of the AC regeneration side high-side floating power supply, whereas the VS pin is the ground of the AC regeneration side high-side floating power supply. The MD6753 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins.

Figure 9-5 is a schematic diagram of the bootstrap circuit that drives the high-side power MOSFET (Q9).

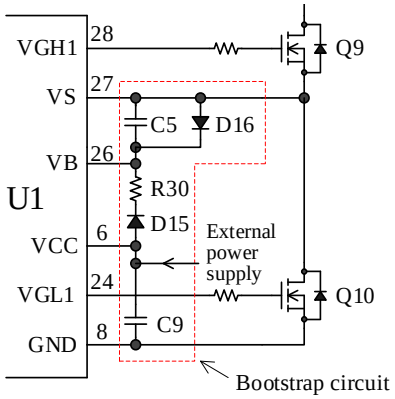


Figure 9-5. Bootstrap Circuit

In the condition where the high-side power MOSFET is turned off and the low-side power MOSFET (Q10) is turned on, the VS pin voltage has almost the same potential as the ground. Then, C5 is charged with the VCC pin. When the voltage between the VB and VS pins (hereafter "VB–VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When VB–VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating (i.e., VB_UVLO). The VB_UVLO protects the IC in case both ends of C5 and D16 are shorted. The bootstrap circuit components must meet the following:

- **D15**

D15 should be a fast recovery diode with a short recovery time and a low reverse current. When the maximum supply input voltage is specified at 265 VAC, it is recommended to use a fast recovery diode with V_{RM} = 600 V.

- **C5, C9, R30**

The values of C5, C9, and R30 are determined by the following parameters: the total amount of gate charges of the external power MOSFETs, Qg; the amount of a voltage dip between the VB and VS pins during operation at the lowest oscillation frequency. C5, C9, and R30 should be adjusted according to voltages measured by a high-voltage differential probe so that VB–VS voltage exceeds $V_{BUV(ON)}$ = 6.8 V. C5 and C9 should be film or ceramic capacitors with a low ESR and a low leakage current. The reference value of C9 is 0.47µF to 1 µF. The time constants of C5 and R30 should be set within 500 ns. C5 should have a capacitance of 0.047 µF to 0.1 µF; R30 should have a resistance of 2.2 Ω to 10 Ω.

- **D16**

D16 is used for protecting the VS pin from having a negative potential. D16 should be a Schottky diode with a low forward voltage so that VB–VS voltage does not fall below −0.3 V of its absolute maximum rating.

9.3. Startup Operation

The power supply voltage for control circuit of the IC is externally applied to the VCC pin that is the power input pin. When the AC power supply is turned on and the VCC pin voltage applied from the external power supply reaches $V_{CC(ON)}$ = 11.0 V or more, the power MOSFETs start oscillating and the output voltage rises. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.3 V or less, the IC stops operation by undervoltage lockout (UVLO) circuit.

9.4. AC Power Supply Input Undervoltage Lockout, AC Power Supply Input Off-state Detection Function

The IC incorporates the AC power supply input undervoltage lockout and the AC power supply input off-state detection function. These functions allow the IC to stop the switching operation of the all power MOSFETs when a low AC line input voltage is detected, thus preventing from excessive input current and overheating.

Figure 9-6 shows the VSENx pin peripheral circuit.

The VSENx pin monitors the AC input voltage. Each protection starts operating when either of the two conditions persists for its own fixed delay time: when the AC input voltage falls below its normal-state level and $V_{SENx} \leq V_{SEN(OFF)}$ of 0.47 V; or when V_{SENx} stays unvaried. In either condition, the IC stops all power MOSFETs switching operation after a lapse of $t_{VSEN(OFF)}$ = 10.0 ms (i.e., the AC power supply input undervoltage lockout), or the GPIO04 pin becomes logic low after a lapse of $t_{VSEN(AC\_OFF)}$ = 23.0 ms (i.e., the AC power supply input off-state detection function). When all the following conditions are met, all power MOSFETs resume switching operation according to output load: the AC input voltage is rising, the IC is in operation, and $V_{SEN} \geq V_{SEN(ON)}$ of 0.56 V.

The reference resistances of R17 and R22, the resistor to be connected to the VSENx pin, is about 20 kΩ. R13 to R22 should be selected based on the operation performance checked with an actual board. R13 to R16 and R18 to R21 are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; connect these resistors in series to reduce each applied voltage.

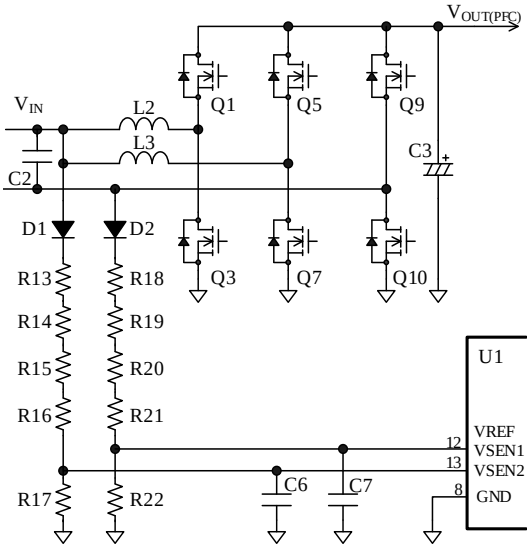


Figure 9-6. VSENx Pin Peripheral Circuit

9.5. VCC Pin Overvoltage Protection

When the voltage between the VCC and GND pins increases to$V_{CC(OVP)}$ = 19.0 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. Then, the IC stops switching operation of all power MOSFETs. After that, when the Protection Recovery Time, t_{AR} = 3000 ms or more, elapses, the IC releases the VCC_OVP operation and restarts to operate. When the causes of the overvoltage condition are eliminated, the IC automatically returns to normal operation.

9.6. Overcurrent and Overload Protection

The IC has the overcurrent protection (OCP). The current flowing to the power MOSFETs of the PFC stages are detected by each current trance. The detected low-side signals of Q3 and Q7 are input to the CS1 pin. The detected high-side signals of Q1 and Q5 are input to the CS2 pin. When the AC input voltage is positive, the overcurrent through the PFC circuit is detected by the CS1 pin. When the AC input voltage is negative, it is detected by the CS2 pin.

This function monitors the CSx pin voltage on a pulse-by-pulse basis, and limits the on-time of the main power MOSFETs for PFC control when the CSx pin voltage reaches the OCP threshold voltage. The OCP threshold voltage has a range shown in Figure 9-8.

As shown in Figure 9-7, when the number of the half-wave cycle of the AC input voltage with the OCP state (i.e., the CS pin voltage exceeds the OCP threshold voltage) becomes more than the fixed number of times, $N_{OPP(AC)}$ = 32 times, the overload protection (OLP) is activated to stop the oscillation operations of the all power MOSFETs. When the Protection Recovery Time, t_{AR} = 3000 ms or longer, elapses after that, the IC releases the OLP operation and restarts to operate. When the causes of the overcurrent condition are eliminated, the IC automatically returns to normal operation.

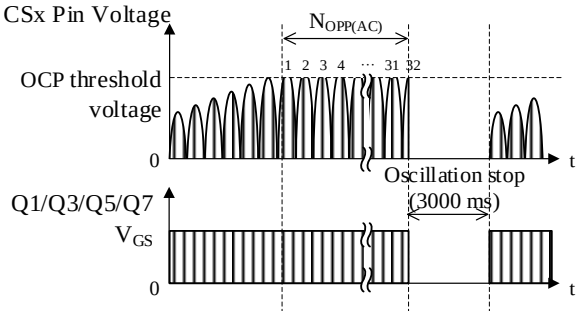


Figure 9-7. OCP and OLP Operational Waveforms

In all AC input voltage specifications, the current transformer should be set so that CSx pin voltage stays within the range shown in Figure 9-8. The winding number ratio of the current transformer, n, is calculated as follows:

$$n = \frac{I_{D(PEAK)}}{V_{OCP}} \times R_{CS} \quad (2)$$

Where:

$I_{D(PEAK)}$ is the drain current in the PFC_OCP operation,

R_{CS} is the current detection resistance of the current transformer (i.e., R11 in Section 6), and

V_{OCP} is the OCP threshold voltage.

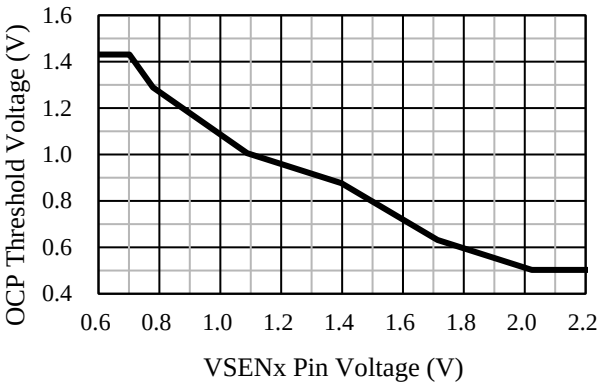


Figure 9-8. OCP Threshold Voltage vs. V_{SEN} Pin Voltage (Peak)

9.7. Overvoltage Protection for Output

The VREF pin detects an overvoltage condition of the output. Figure 9-9 shows the waveforms of Overvoltage Protection (OVP) operation. When the VREF pin voltage increases to $V_{REF(OVP)}$ = 2.352 V or more, the OVP is activated to stop all power MOSFETs to avoid a further increase in the output voltage. When the VREF pin voltage decreases to $V_{REF(OVP\_R)}$ = 2.297 V or less along with a lowering in the output voltage, all power MOSFETs resume oscillating. In this way, the intermittent operation is repeated while the output overvoltage condition persists. When the causes of the overvoltage condition are eliminated, the IC automatically returns to normal operation.

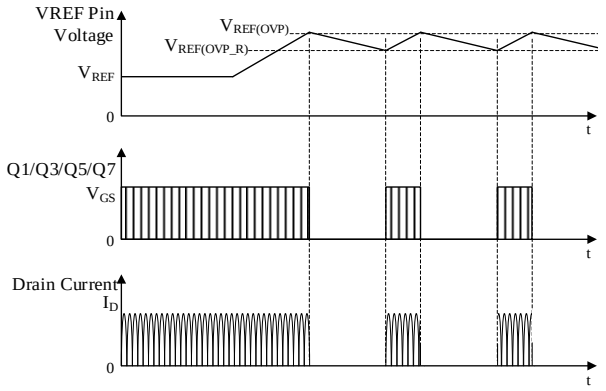


Figure 9-9. OVP Operational Waveforms

9.8. Undervoltage Protection for Output

The VREF pin also detects an undervoltage condition of the output. Figure 9-10. shows the waveforms of the undervoltage protection (UVP) operation.

When the VREF pin voltage decreases to $V_{REF(UVD)}$ = 2.088 V or less, the on-time of the main power MOSFETs for PFC control is lengthened.

When the AC input voltage is positive, the main power MOSFETs for PFC control are Q3 and Q7 of low-side. When the AC input voltage is positive, they are Q1 and Q5 of high-side.

Besides, when the VREF pin voltage still decreases to $V_{REF(UVP)}$ = 1.103 V or less, the UVP is activated to stop all power MOSFETs oscillation. When the VREF pin voltage decreases even further to $V_{REF(UVP\_R)}$ = 0.552 V or less after that, all power MOSFETs resume oscillating.

During the non-oscillating period of the power MOSFETs, if the VREF pin voltage does not go below $V_{REF(UVP\_R)}$ within $t_{(UVP\_R)}$ = 819.2 ms, all power MOSFETs resume oscillating at the time that $t_{(UVP\_R)}$ elapses. In this way, the intermittent operation is repeated while the output undervoltage condition persists. When the causes of the undervoltage condition are eliminated, the IC automatically returns to normal operation.

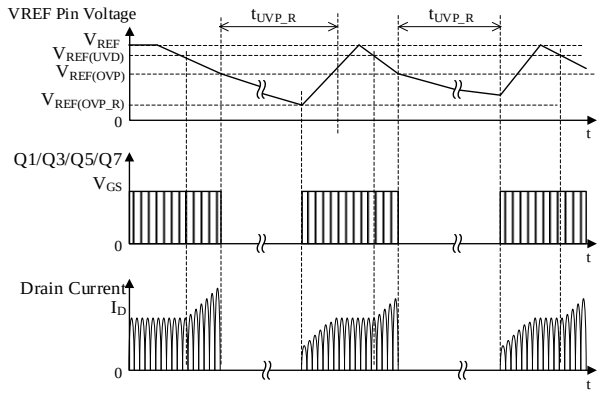


Figure 9-10. UVP Operational Waveforms

9.9. Thermal Shutdown

When the control circuit temperature reaches $T_{J(TSD)}$ = 125 °C (min.) the thermal shutdown (TSD) is activated. The IC then stops switching operation. In the condition where $V_{CC} \leq V_{CC(P.OFF)}$ of 8.3 V and the control circuit temperature falls below $T_{J(TSD)}$, the TSD circuit is activated again. During the TSD operation, the IC stops its operation. When the causes of the overheating condition are eliminated, the IC automatically returns to normal operation.

10. External Components

10.1. Inductor

Apply proper design margin to temperature rise or magnetic saturation due to copper loss and iron loss.

10.2. Power MOSFET

Use a power MOSFET with a breakdown voltage, VDSS, providing enough margin to the output voltage, $V_{OUT(PFC)}$. Choose a proper size of heatsink that takes switching and on-resistance losses due to power MOSFETs into account.

10.3. Output Capacitor (C3)

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

11. PCB Pattern Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. Thus, to reduce the impedance of the high frequency traces on a PCB (see Figure 11-1), they should be designed as wide trace and small loop as possible. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

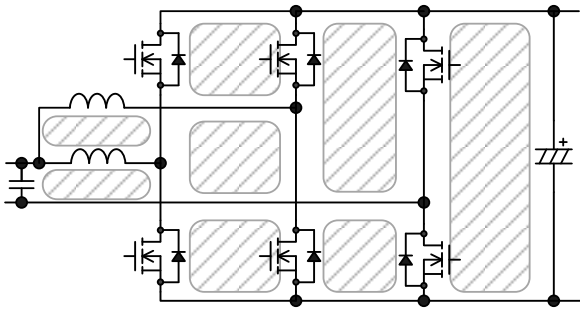


Figure 11-1. High-frequency Current Loop

Figure 11-2 is a peripheral circuit example of the IC. The following considerations should be taken into account in designing pattern layouts for your application.

1) Main Circuit Trace Layout

Trace where switching currents pass through should be as wide and looped small as possible.

2) Logic Ground Trace Layout

If a large current flows through a logic ground, electric potential across the logic ground may vary and thus cause the IC to malfunction. Ground traces should be as wide and short as possible.

Logic ground traces should be designed as close as possible to the GND pin, at a single-point ground (or star ground) that is separated from the main circuit. Do not connect the PGND pin to these traces. Traces of the ground (i.e., the capacitors of the GND, PGND, and VCC pins) should be separately connected at a single-point ground whose connection is configured to the root of the output capacitor C3 in the PFC stage.

3) Peripheral Connections to VCC Pin

Traces connected to the VCC pin should be looped small as possible as the pin supplies power to the IC. Connect the film capacitor C9 (about 0.1 μF to 1.0 μF) between the VCC and GND pins with a minimal length of traces.

4) Peripheral Connections to VB Pin

The components of the bootstrap circuit connected between the VCC and VB pins (D15, R30) should be placed as close as possible to the IC. The capacitor C5 connected between the VB and VS pins should also be placed with a minimal length of traces.

5) Components for Logic Control System

These components should be placed close to the IC, and be connected to the corresponding pin of the IC with a minimal length of traces.

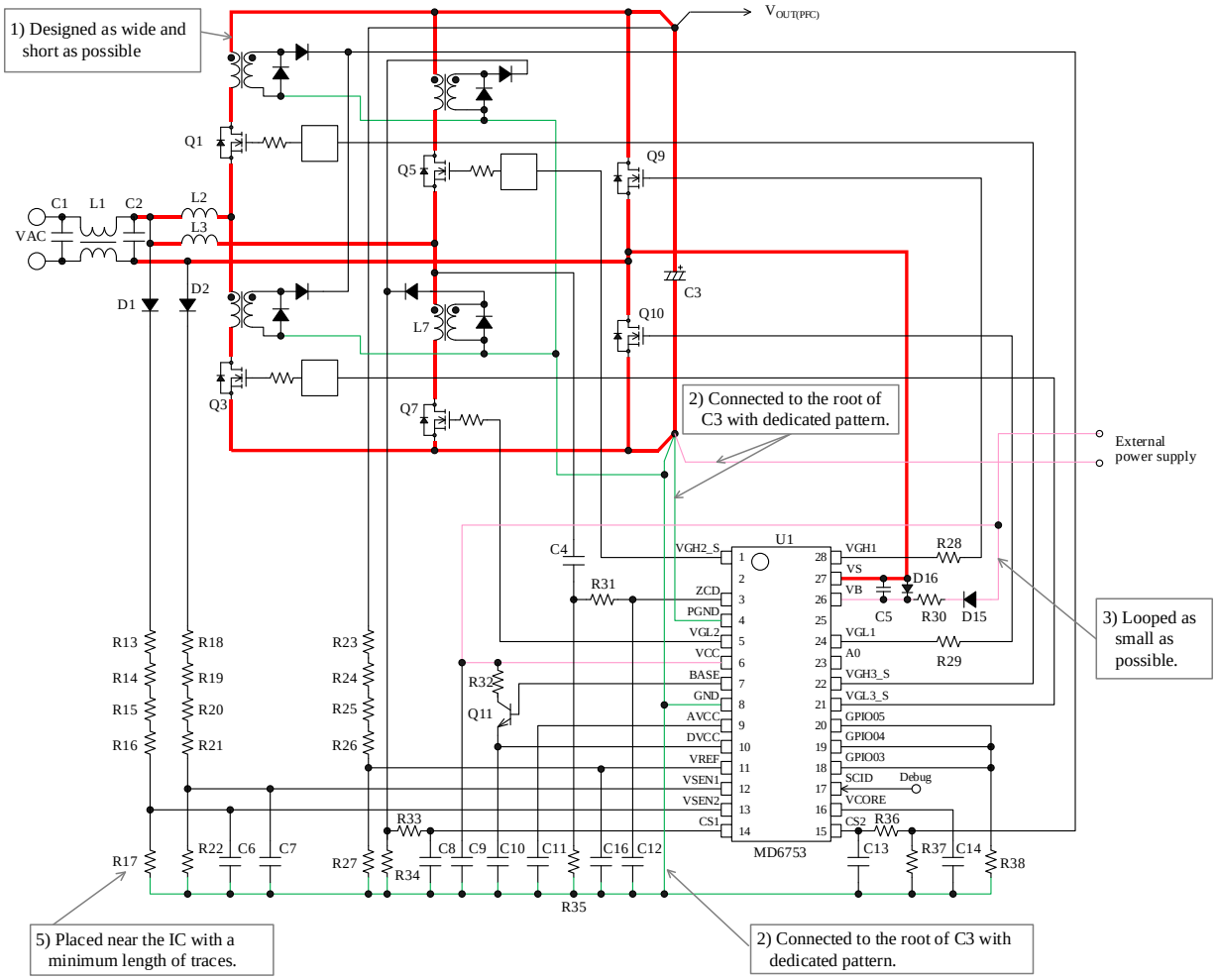


Figure 11-2. Example Connections to IC and Its Peripheral Circuits

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